Spacing of High-Brightness LEDs on Metal Substrate PCB's for Proper Thermal Performance

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Abstract

High brightness Light Emitting Diodes (LEDs) are appearing more frequently in lighting applications. As these LEDs are used and planned for more general lighting systems, more emphasis is placed on locating these high power package systems in close proximity to each other to produce high lighting levels. This close packing can take the form of locating level 1 packages next to each other or locating chip-on-board (COB) LEDs next to one another. This leads to the question of how close can the LEDs be placed by the circuit board designer, and there has been little published work to show what spacing is possible in multiple LED systems. The spacing issue is also affected by the type of printed circuit board (PCB) used, which is normally a composite made up of a thin PCB bonded to a relatively thick metal substrate (a metal core PCB - MCPCB). The variables of dielectric, copper and solder layer thicknesses result in different proximities possible for LED spacing, and are especially critical for COB applications. This paper explores the spacing and placement of LEDs in tight array for 1-watt class devices using a design of experiments (DOE) methodology for analytical computations.

Keywords

High brightness, LED, LED layout, thermal management, optimum spacing

Introduction

With the introduction of blue LEDs in the mid-1990's, the goal of creating general illumination white LED lighting was finally possible. Phosphors were created that allowed some of the blue light to be converted to yellow and the mix created white light. The first white LEDs were created in the standard LED indicator-style lamps of the era, such as the T 1 ¾ (5mm) or T1 (3mm) level 1 (L1) devices. However, the low level of light output from the small die (around 1-2 lumens) coupled with the poor thermal performance of the standard packages (~350°C/W) limited the usefulness of the LEDs toward the goal of general illumination.

The luminous efficiency of LEDs has also risen to a certain level and is now only slowly increasing. At first, gains were made in efficiency so that 20 lumens/watt (LPW) were achieved quickly. Efficiency has slowly risen in the last few years to around 30 LPW, and trends indicate 50-60 LPW will occur in the next few years. But with general illumination sources requiring light output measured in hundreds and thousands of lumens, this meant large amounts of wattage would be used. This necessitated L1 devices having thermal resistances much lower than hundreds of °C/W, and the development of thermally efficient power packages for LEDs began. Through the last few years, package thermal resistance has improved to around the 10°C/W level, and LEDs have in turn increased power dissipations from less than 100 mW to a 1-5 W range, allowing L1 devices with 20 to 100 lumens of output to be developed. L1 devices in this range are suitable for developing early general illumination systems. The challenges associated with managing the thermal output of the LEDs has been discussed in recent years [1-3].

For comparison with typical lighting sources in use today, Table 1 shows the typical luminous efficiencies of various lighting sources.

By examining this table, one can see that LEDs are now efficient enough to replace incandescent lamps, although adoption is occurring slowly due to cost issues and return on investment. Additionally, LED lighting systems cause a major shift in how waste heat must be removed – conduction now becomes the dominant method. Radiation is not viable as the major path as it is for other types of lighting. It is this shift to conductive cooling that means parameters that this paper investigates – LED location, material geometries and material properties – become significant to understand and design for effective LED cooling.

Light source	Luminous efficiency, LPW	Heat lost by radiation, %	Heat lost by convection, %	Heat lost by conduction, %
Incandescent	10-20	>90	<5	<5
Fluorescent	75-90	40	40	20
High Intensity Discharge	100-120	>90	<5	<5
LED	30-35	<5	<5	>90

Table 1: Comparison of typical lighting sources with LEDs

Still, with this output for L1 devices, general illumination systems require multiple LEDs, if not large arrays. Single LED systems are straightforward to analyze,

but when multiple LEDs are used more forethought must be given to how to place the LEDs together. It is favorable to make light sources compact, so arranging LEDs in a close array is generally a desirable goal but also the one most likely to create temperature issues for the LEDs. This paper will analyze a typical two-dimensional array of LEDs in a typical mounting method to determine some design guidelines and explore sensitivities of various factors, and do so for a L1 package called chip-on-board (COB).

High Power LED Packaging Methods

With the introduction of high power L1 devices, ordinary printed circuit boards (PCBs) were not adequate to remove the generated heat. This is because the power packages use a low resistance conduction path and need to sink the waste heat into a very low thermally resistant conductive path. This has led to the standard use of a metal substrate PCB under power package devices.

These metal substrate boards are normally composed of a thick metallic layer (usually aluminum alloy sheet such as 6061), around 1.6mm, with a thin PCB circuit layer laminated on top. The laminated layers are composed of a dielectric (to form an electrical barrier to the metallic substrate), a copper layer (the circuit traces) and a solder layer on the copper (for tinning and component attachment). Other layers such as solder masks are also employed but these are not found under the heat generating components [4].

Soldered to these metal core PCBs (MCPCBs) will be the various electrical circuit components and the LEDs. The L1 devices themselves may be of different designs. Some of the power packages are somewhat traditional in that they have a lead frame, a cup where the LED is mounted, a plastic lower housing and a clear lens upper housing. But there are also methods of mounting a LED device directly to a MCPCB without using the lead frame and various plastic parts. This direct chip-on-board mounting offers some advantages but also means the LED chips can be mounted even closer to each other than the more traditional lead frame power packages, exacerbating the thermal issues.

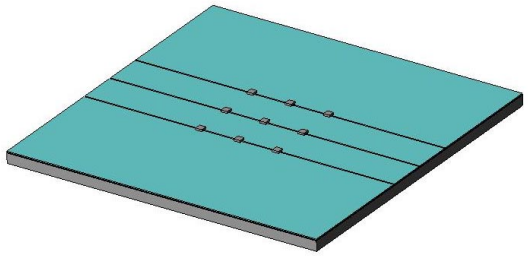
Analytical Model: 2D COB Array

A solid model assembly of a MCPCB and nine LEDs was constructed using SolidWorks software. The model was parametrically constrained so that the nine LEDs could be moved in and out with a single dimensional change, with only the middle LED fixed in the 3x3 array. The LEDs themselves were modeled as solid bricks, as one method to easily make an LED is to create a volume and adjust the thermal conductivity so that the maximum temperature on the top surface of the volume mimics the LED junction temperature. This effectively creates a "compact model" of a LED.

Figure 1 shows the baseline model, with the LEDs spaced at 6.2mm (center to center). Figure 2 shows the same model with one dimension changed, so the LEDs are spaced at 1.7mm. Figure 3 is a close up view of the LED array in the 1.7mm spacing configuration. The 6.2mm configuration is representative of the closest one can space some typical power packages (dies packaged with lead frames and plastic), and the 1.7mm represents a suitable close spacing for chip on board applications.

The LEDs in this model are electrically arranged in a 3x3 series/parallel electrical array. Such arrays are typical in multiple LED circuits to account for forward voltage (Vf) variations between the LEDs and ensure a reasonable current distribution. This also determines the copper layer arrangement of the MCPCB and how the heat distributes through the various layers of the MCPCB. Additionally, the top surfaces of the LED parts received one watt of input power each.

Figure 1: LED Model with Maximum Spacing (6.2mm) on MCPCB



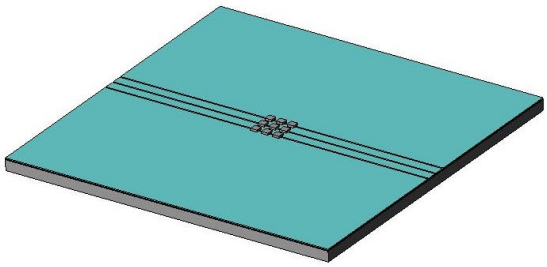


Figure 2: LED Model with Minimum Spacing (1.7mm)

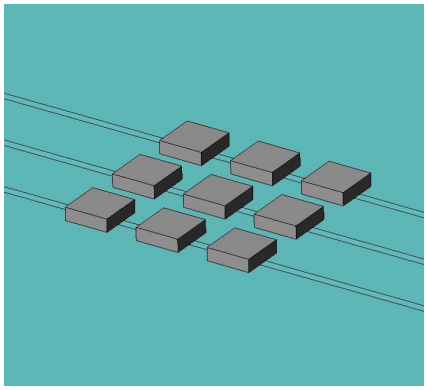


Figure 3: Close View of Minimum LED Spacing (1.7mm)

Parameter	Units	Lower Bound	Upper Bound
LED Spacing	mm	1.7	6.2
Dielectric Thickness	mm	.1016 (.004in)	.2032 (.008in)
Copper Thickness	mm	.01778 (1/2 oz)	.07112 (2 oz)
Solder Thickness	mm	.0762 (.003in)	.254 (.010in)
Temperature BC	°C	20	40

Table 2: Parameter Listing and Ranges

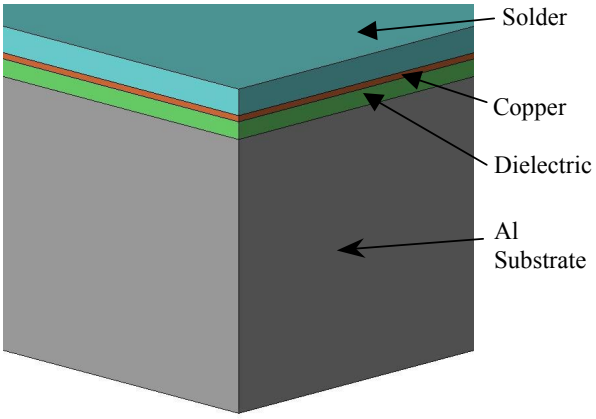


Figure 4: MCPCB Layers

Material	Thermal Conductivity (W/m-°K)
Aluminum	144 (0°C) – 165 (100°C)
Dielectric	2.2
Copper	401
Solder	35
LED model	21

Table 3: Material Thermal Conductivities

The various layers of the MCPCB were explicitly modeled and shown in Figure 4. The thick bottom layer is the aluminum substrate; next up from that layer are the dielectric, copper and solder (tinned) layers. The solder layer is assumed to cover all the exposed copper, and no solder mask is modeled.

In this analysis, the parameters varied for response functions are the LED spacing, the dielectric layer thickness, the copper layer thickness, the solder layer thickness and the boundary condition temperature on the underside of the aluminum substrate (held at a constant temperature). Table 2 lists these various parameters, and Table 3 lists the thermal conductivities of the various materials used for this analysis. In addition, the finite element solution (performed using ANSYS Design Simulation software) was solved using a 5% convergence value.

Design of Experiments Method

Design of experiments (DOE's) offer some key advantages over typical experimentation methods when several variables are under investigation. In research, experimental parameters are often varied one factor at a time (OFAT) while holding other parameters fixed. In the past, this has been thought to be adequate to understand the effect of the parameter on the system. However, this usually does not allow an optimum solution to be identified, nor does it allow parameter interactions to be explored, in cases where varying one parameter can cause a second paramter to affect the system differently [5]. As a result, the goal of optimizing an output, such as heat transfer, may not be realized by the OFAT approach, whereas the DOE process allows for optimization to be predicted even if the experiment was not conducted at the exact parameters.

Additionally, a properly constructed DOE can map out transfer functions and response surfaces with fewer experimental runs than any other methodology. The resolution between the variables is determined by the type of DOE setup that is chosen, and the higher resolution DOE's allow less "confounding" or indistinguishability between combinations of variables. For example, a DOE matrix that is called full factorial is a complete matrix that provides information about how each parameter affects the system (such as A, B, C, etc.) and also provides all the affects of the parameter interactions (AB, BC, AC, ABC, etc.). This is the largest DOE and also the most complete.

Below full factorials, an experimental matrix can be chosen that allows fewer experiments but at a cost of confounding. Often that is not an issue with physical systems, as two parameter interactions are usually the most complex found in the system. For this type of DOE, the matrix allows confounding of three parameter interactions with single parameters, and in some cases two parameter interactions with single parameters. As an example, this could mean the interaction of ABC is indistinguishable from paramater's C influence on the system. Thus an experimenter must decide how much confounding between terms to allow, based on the physics of the problem and past experience. Once a resolution level is chosen, the DOE matrix provides the fewest number of experimental setups to create the transfer function, which describes the behavior of the system. Thus a DOE not only provides the best information about a system, but also does so most economically [6].

For this analysis, the five factors were organized into twenty-seven different analysis runs by using the ANSYS DesignXplorer software. This is a DOE-type of software add-on that uses the Design Simulation model and analysis engine to solve each analysis run. The DOE matrix is automatically generated by the software, and DesignXplorer assumes the factors will produce a system quadratic effect (it evaluates each variable at five levels), as well as assuming no significant three-way interactions are present. The data from these runs were exported to DOE KISS [7], a design of experiments software, for determining the transfer function and other results.

Results

The twenty-seven analysis runs produced a good fidelity regression model for the final result. Using standardized coded values (each parameter is standardized to a range of –1 to 1), the following transfer function resulted using the DOE KISS software:

$$(1)\quad Tmax = 61.0 + 4.74*A - 2.63*B + 0.922*C - 1.15*D + 0.346*E + 1.49*B^2$$

where Tmax is the maximum temperature of the center LED of the array (°C), A is the boundary condition temperature, B is the LED spacing, C is the dielectric thickness, D is the copper thickness, and E is the solder thickness. This transfer function is a predictive model based on fitting the analytical experiments to a function with linear coefficients. Even if a particular combination of parameters wasn't analyzed, this temperature function model can reasonably predict it.

From this model it can be seen that no significant parameter interactions occurred (e.g., no AB, BC, etc., terms). The LED spacing does occur as a linear (B) and a quadratic (B^2) term, and this comes about from its affect on Tmax as the spacing becomes very close. This regression fit is of good fidelity as the R^2adj term is 95.8%.

To see how much each factor contributes to the maximum LED temperature, one can look at the coded coefficients and/or the plots of mains effects (the A, B, etc. parameters). This gives a relative idea of how each variable affects the end results compared to other variables – which one has a greater effect. Figure 5 shows the mains effects for the five variables generated by the DOE KISS software. From this, one can see that the boundary condition temperature is still the primary driving force of the maximum LED temperature (the absolute value of the slope is qute high). However, as one spaces the LEDs close together, this term begins to dominate the temperature rise and can cause a significant rise in the LED temperature. This is seen by the quick rise in the slope of the LED spacing curve from 2.825mm to 1.7mm. For systems made with MCPCBs such as this one, and one watt dissipating LEDs, this rapid temperature rise begins to occur at a spacing of 2.825mm. This information is crucial to system designers who need to know how close the LEDs can be spaced together before seeing significant adjoining heating effects.

The other factors in the MCPCBs can change the maximum LED temperature but only vary them at secondary levels – factors of five to ten times less impact. The LED spacing also becomes secondary once the spacing reaches approximately 3mm. The reasons these are only secondary effects can be seen in the temperature gradients produced in the system. Figure 6 shows the nine LED array spaced out near maximum separation, and the heating zones produced by each LED is fairly small – on the order of 1 to 2 mm. The heat produced by the LED is sunk into the solder layer first, and some spreading out beyond the device occurs here. Once a larger area of 4 to 5mm diameter is reached, the area through the MCPCB layer system is now large enough to allow easy movement of the heat (the increased area lowers the path thermal resistance to a low enough level).

From this, one can see that if LEDs must be tightly spaced together, some of these secondary factors can be used to mitigate the LED temperature rise. Thinner solder layers are best, as are thicker copper traces. These layers primarily affect the heat spreading from the LED. The next part of the thermal path is the dielectric layer, and thinner is better here as this layer is primarily a resistance driven by the layer thickness. When the heat is finally conducted into the aluminum substrate, the aluminum is adequate to move the heat to the boundary condition based on the area of heat conduction under each of the LED zones.

These effects are seen in the other figures. Figure 7 shows a close view of the widely spaced LEDs and the heating zones. By changing the contour scale, Figure 8 shows how the heating zones are beginning to affect each other at this distance, although the effect is minimal compared to the closer 1.7mm spacing. Figure 9 shows the heating zone under the highest temperature LED, as it spreads from the square pattern of the LED into a round spreading zone in the top and underlying layers of the MCPCB. Finally,

Figure 10 shows the temperature map of the closest LED spacing at 1.7mm.

Conclusions

For COB LED applications, the temperature of the MCPCB is still the most important factor in determining the maximum LED temperature for widely spaced LED arrays. Once the array is spaced below a critical value, the heating zones of each LED intersect and the reduction in area causes an increase in the system thermal resistance for the array. For a typical MCPCB, a 1-watt class LED has a zone of approximately 4-5mm in diameter and LEDs spaced closer than this will see a rise in temperature, sharply so below 3mm spacing. The dielectric, copper and solder layers of the MCPCB can offset this temperature rise to some degree, but these only provide a secondary level of temperature relief and cannot overcome the primary boundary condition and LED spacing factors.

References

[1] Petroski, J., *Thermal Challenges Facing New Generation LEDs for Lighting Applications,* SPIE Proceedings Vol 4776, 2003, pp 215-222.

[2] Arik, M., et al., *Thermal Management of LEDs: Package to System,* SPIE Proceedings Vol 5187, 2002, pp 64-75.

[3] Arik, M., et al., *Thermal Challenges in Future Generation Solid State Lighting Applications: LEDs,* Thermal and Thermomechanical Phenomena in Electronic Systems, ITHERM 2002, pp 113-120.

[4] As an example, see Bergquist Company T-clad MCPCB construction at www.bergquistcompany.com

[5] Schmidt, S., and Launsby, R., Understanding Industrial Designed Experiments, 4th edition, Air Academy Press, CO, 2000, pp 1-9 to 1-11.

[6] Ibid,. chapter 3.

[7] *DOE KISS* software is a DOE software program that runs within Micosoft Excel, copyright 1997 Digital Computations and Air Academy Press.

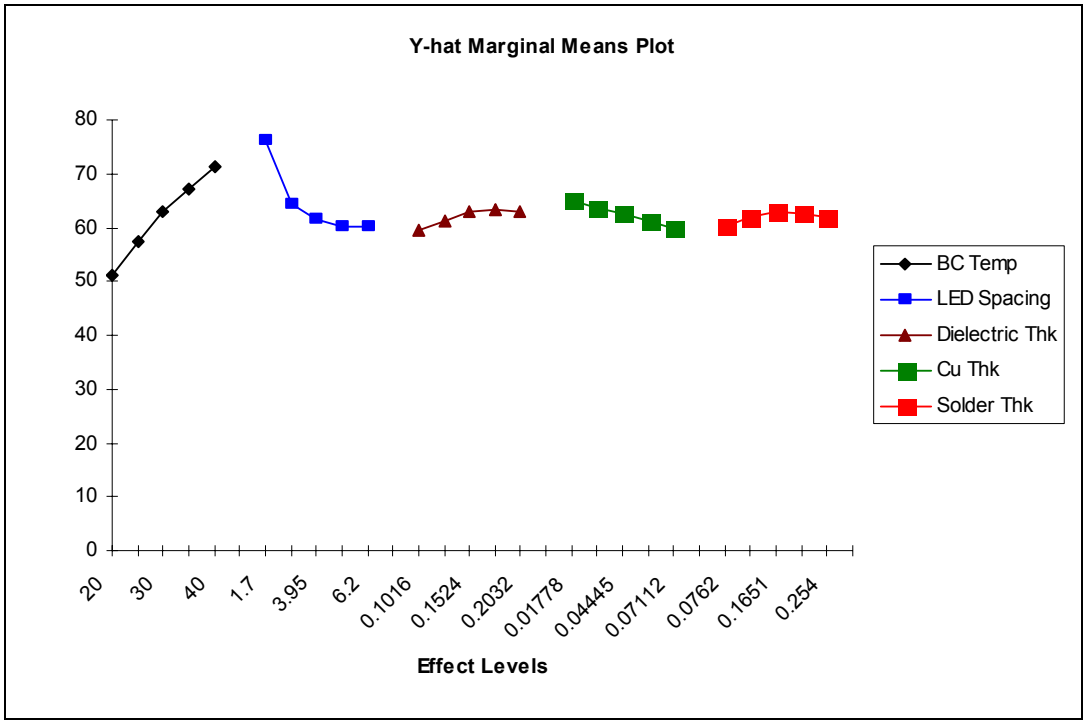


Figure 5: Mains Effects Plot for Parameters, showing LED spacing dominating temperature rise at close values

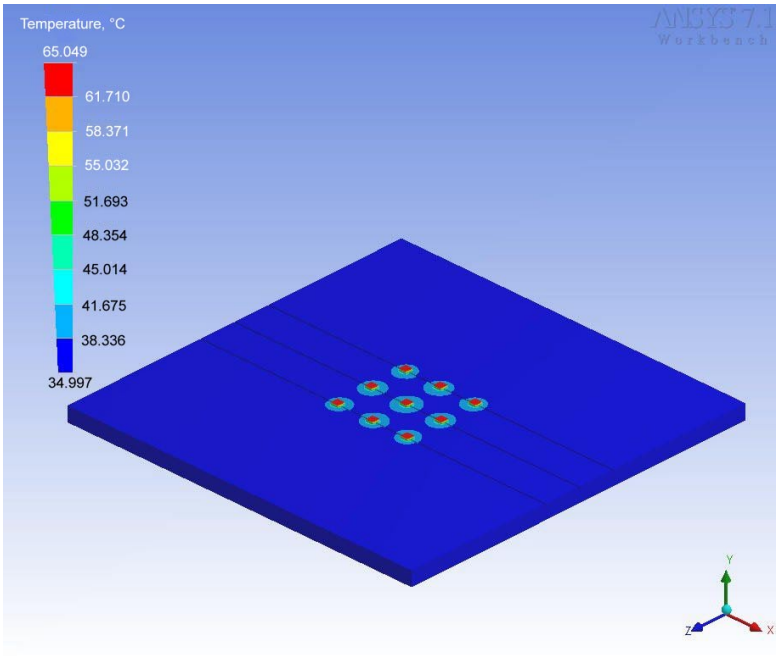


Figure 6: Temperature Results, Maximum LED Spacing (6.2mm)

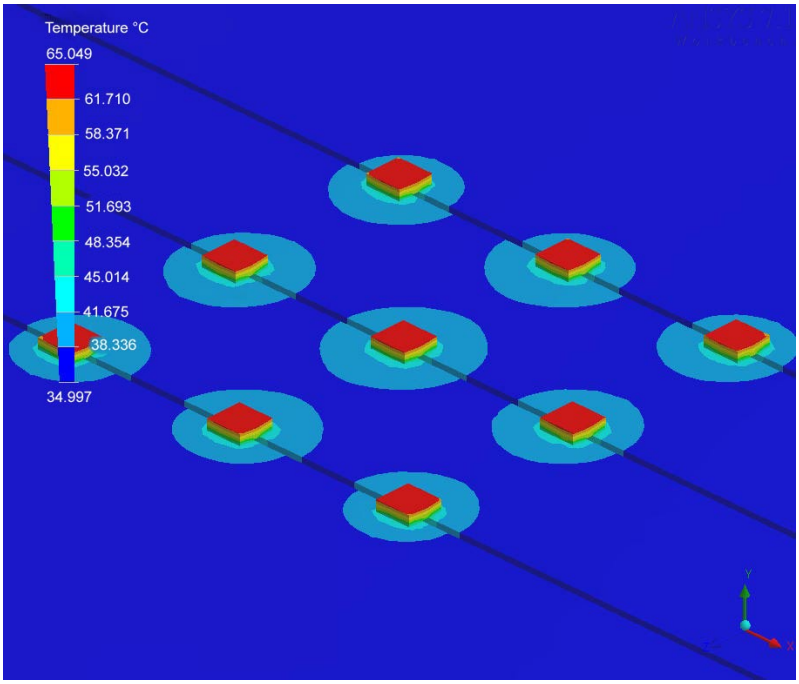


Figure 7: Heating Zones around LEDs at Maximum spacing (6.2mm) showing little interaction

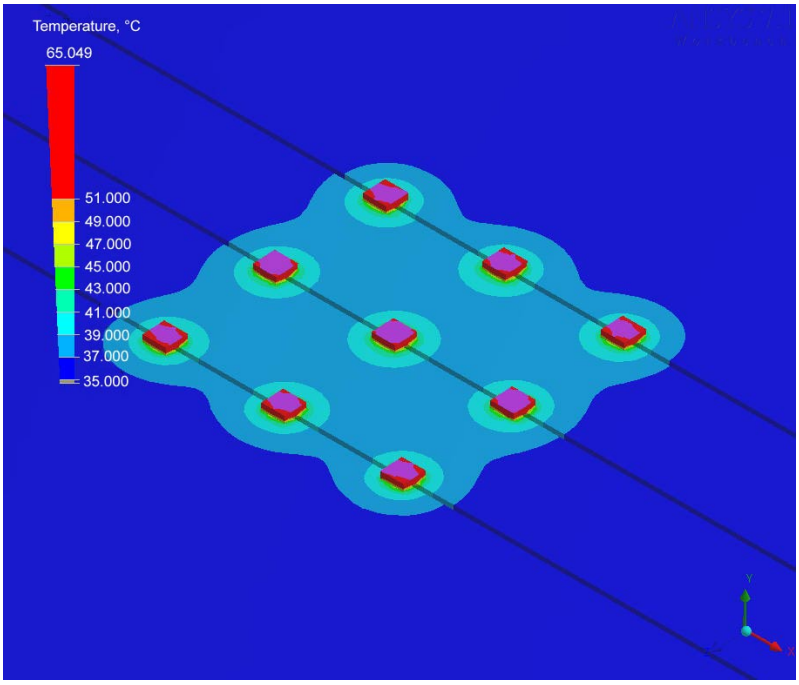


Figure 8: Scale Change, Showing the Lightly Affected Zone Caused by LED Heat Dissipation

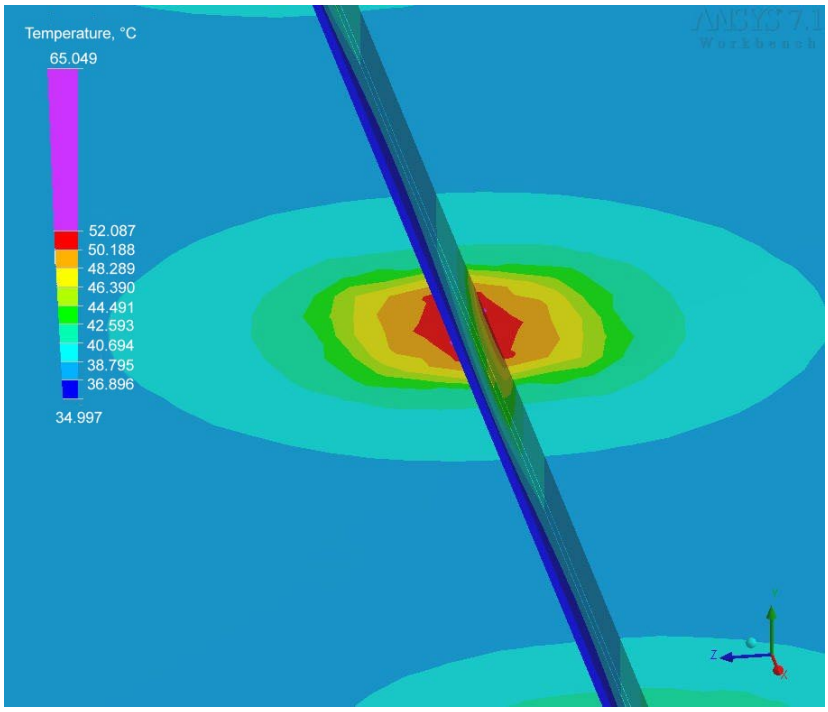


Figure 9: Heating Zone under LED Transitioning from Square to Round Zone

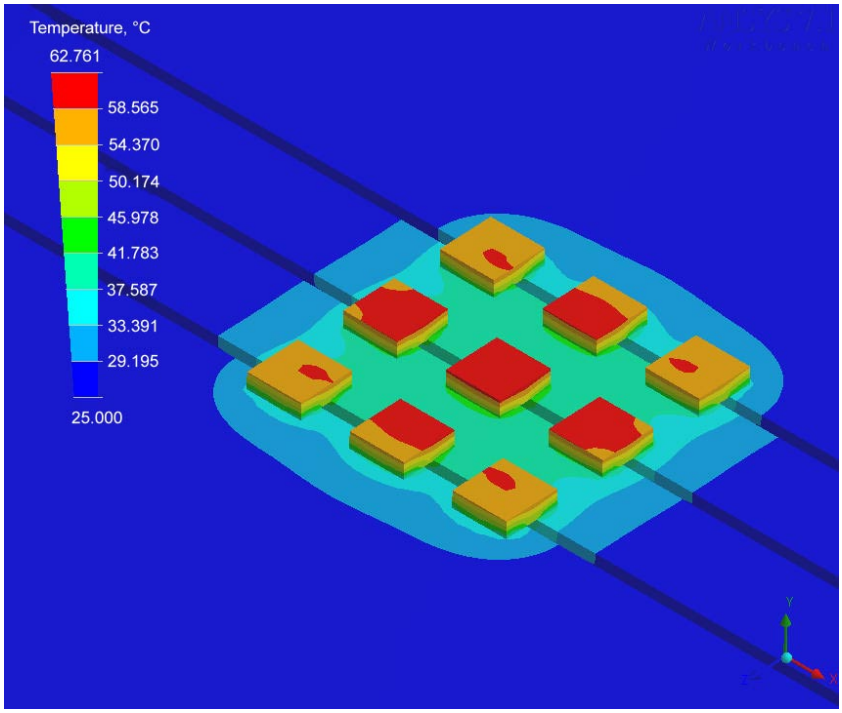


Figure 10: Close LED spacing (1.7mm) Heating Zones (note ambient temperature in this case is 25°C not 35)